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EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/725,730	SERRANO ET AL.	
	Examiner	Art Unit	
	Edward J. Dudek	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/19/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the amendment filed in application #10/725730 on 19 March 2007.

Claims 1-30 have been cancelled.

Claims 31-50 have been added and are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 34, 37, and 39-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 34 recites the limitation "the plurality of memory operations" in line 2. There is insufficient antecedent basis for this limitation in the claim. For the remainder of this Office Action this limitation will be construed as "the plurality of instructions".

Claim 37 recites the limitation "the criteria" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 39 recites the limitation "the address information" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claims 40-45 are also deficient as they depend from claim 39.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 39-45 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 39 is directed to storing information about instructions that have been executed by a processor. This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete, and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having a real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for gathering specific information regarding the instructions that have executed on the processor. Then making a determination about a relationship among the data stored in the buffer. There is no real world result than can be realized from this. Therefore, the produced result remains in the abstract and, thus, fails to achieve the required status of having a real world value.

Claims 40-45 are also deficient as they depend from claim 39.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talcott et al (U.S. Patent Application Publication #2003/0188226) in view of Gonzales et al (U.S. Patent #5,488,688) and Wu ("Value-Profile Guided Stride Prefetching for Irregular Code").

As per claim 31: Talcott discloses a processor comprising: an execution unit, the execution unit to execute instructions (see [0017]); and to store data regarding a plurality of instructions executed by the execution unit (see [0019]), wherein the data stored for each executed instruction includes an instruction address and an effective address for the executed instruction (see [0029]). Talcott fails to disclose storing information in a buffer and halting the storing of information in the buffer upon the occurrence of an event. Gonzales discloses a data processor with real time diagnostic capability (see abstract). Gonzales teaches a buffer that gathers information about the software instructions that have been executed by the processor, and then when an event condition is encountered the FIFO is halted (see column 3, lines 39-54). Halting the FIFO allows the data in the FIFO to be examined without having to stop the system from executing instructions (see column 3, lines 39-54). It would have been obvious to

a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Talcott to store the gathered information in a buffer and to halt the storage of information in the buffer upon encountering an event condition, as disclosed by Gonzales, to allow the system to examine the contents of the FIFO without having to stop the system from running, as disclosed by Gonzales. The combination still fails to disclose determining a relationship between a set of memory operations based at least in part on the stored address information for the memory operations. Wu discloses monitoring memory operations to increase the performance of software running on a processor (see abstract). Wu monitors memory accesses to determine the stride value, and then inserts a pre-fetch instruction to increase the performance of the processor (see page 309, paragraph 1). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the combination of Talcott and Gonzales to include determining a relationship among a set of memory operations, as disclosed by Wu, to allow memory accesses with certain stride values to be pre-fetched, thereby increasing the performance of the processor, as disclosed by Wu.

As per claim 32: determining a base address for each set of executed instructions (see [0029]).

As per claim 33: the buffer comprises a circular buffer (see Gonzales column 3, lines 39-54, *since the FIFO is implemented in hardware, the FIFO will have a fixed capacity since any type of hardware will have a limited area for storage, therefore it is*

equivalent to a circular buffer. Once the FIFO reaches capacity the oldest entries will be overwritten each time another entry is stored in the buffer).

As per claim 34: further comprising a filter, the filter determining whether the execution of each of the plurality of memory operations meets a criterion for storage (see [0008]).

As per claim 35: the filter criterion is based upon whether the instruction is a stack memory access; whether an instruction address is within an address range; whether an effective address is within an address range; whether data latency is within a latency range (see [0028]); wherein a memory operation loads or stores a pointer value (see [0029]-[0030], *the effective address is for memory operations involving loads or stores*).

As per claim 36: wherein the event comprises a miss in a cache (see [0008]).

As per claim 37: wherein the criteria include one or more of an invalid effective address or an address that matches a particular range of addresses (see [0028]).

As per claim 38: the buffer is part of performance monitoring hardware to monitor processor operations to provide data points regarding the executed loads to software (see [0017]).

As per claim 39: Talcott discloses a method comprising monitoring the execution of a plurality of memory operations by a processor (see [0017]-[0019]); storing information regarding the execution of the plurality of memory operations (see [0019]), the address information including an instruction address and an effective address (see [0029]). Talcott fails to disclose storing information in a buffer and halting the storing of

information in the buffer upon the occurrence of an event. Gonzales discloses a data processor with real time diagnostic capability (see abstract). Gonzales teaches a buffer that gathers information about the software instructions that have been executed by the processor, and then when an event condition is encountered the FIFO is halted (see column 3, lines 39-54). Halting the FIFO allows the data in the FIFO to be examined without having to stop the system from executing instructions (see column 3, lines 39-54). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Talcott to store the gathered information in a buffer and to halt the storage of information in the buffer upon encountering an event condition, as disclosed by Gonzales, to allow the system to examine the contents of the FIFO without having to stop the system from running, as disclosed by Gonzales. The combination still fails to disclose determining a relationship between a set of memory operations based at least in part on the stored address information for the memory operations. Wu discloses monitoring memory operations to increase the performance of software running on a processor (see abstract). Wu monitors memory accesses to determine the stride value, and then inserts a pre-fetch instruction to increase the performance of the processor (see page 309, paragraph 1). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the combination of Talcott and Gonzales to include determining a relationship among a set of memory operations, as disclosed by Wu, to allow memory accesses with certain stride values to be pre-fetched, thereby increasing the performance of the processor, as disclosed by Wu.

As per claim 40: the buffer is implemented in hardware (see Gonzales column 4, lines 40-45).

As per claim 41: determining a base address for each set of executed instructions (see [0029]).

As per claim 42: deleting the oldest information in the buffer when new information regarding the execution of a load is stored (see Gonzales Column 3, lines 39-54, *Gonzales teaches using a FIFO as the buffer, therefore by definition the oldest entry would be removed when new entries are added*).

As per claim 43: filtering each of the plurality of memory operations to determine whether to store information regarding execution of the operation in the buffer (see [0028]).

As per claim 44: the event comprises a miss in a cache (see [0008]).

As per claim 45: the criteria include an address that matches a particular range of addresses (see [0028]).

As per claim 46: Talcott discloses a bus (see [0017]); a processor coupled to the bus, the processor comprising: an execution unit to execute instructions (see [0017]); performance monitoring hardware to monitor operations of the execution unit (see [0018]), the performance monitoring hardware to store data regarding each of a plurality of instructions executed by the processor (see [0019), data to include an instruction address and an effective address for each executed instruction (see [0029]). Talcott fails to disclose storing information in a buffer and halting the storing of information in the buffer upon the occurrence of an event. Gonzales discloses a data processor with

real time diagnostic capability (see abstract). Gonzales teaches a buffer that gathers information about the software instructions that have been executed by the processor, and then when an event condition is encountered the FIFO is halted (see column 3, lines 39-54). Halting the FIFO allows the data in the FIFO to be examined without having to stop the system from executing instructions (see column 3, lines 39-54). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Talcott to store the gathered information in a buffer and to halt the storage of information in the buffer upon encountering an event condition, as disclosed by Gonzales, to allow the system to examine the contents of the FIFO without having to stop the system from running, as disclosed by Gonzales. The combination still fails to disclose determining a relationship between a set of memory operations based at least in part on the stored address information for the memory operations. Wu discloses monitoring memory operations to increase the performance of software running on a processor (see abstract). Wu monitors memory accesses to determine the stride value, and then inserts a pre-fetch instruction to increase the performance of the processor (see page 309, paragraph 1). It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the combination of Talcott and Gonzales to include determining a relationship among a set of memory operations, as disclosed by Wu, to allow memory accesses with certain stride values to be pre-fetched, thereby increasing the performance of the processor, as disclosed by Wu.

As per claim 47: the buffer comprises a circular buffer (see Gonzales column 3, lines 39-54, *since the FIFO is implemented in hardware, the FIFO will have a fixed capacity since any type of hardware will have a limited area for storage, therefore it is equivalent to a circular buffer. Once the FIFO reaches capacity the oldest entries will be overwritten each time another entry is stored in the buffer*).

As per claim 48: further comprising a filter, the filter to determine whether the execution of and instruction meets a criterion for storage (see [0028]).

As per claim 49: wherein the event comprises a miss in the cache memory (see [0008]).

As per claim 50: determining a base address for each set of executed instructions (see [0029]).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward J. Dudek whose telephone number is 571-270-1030. The examiner can normally be reached on Mon thru Thur 7:30-5:00pm Sec. Fri 7:30-4 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Edward Dudek
May 8, 2007

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